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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/091,934 | 03/06/2002 | Amir Alon | IL920020007US1 | 7058 |

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| EXAMINER | |
|---|---|
| LEVIN, NAUM B | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2825 | |

DATE MAILED: 08/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/091,934 | ALON ET AL. | |
| | Examiner | Art Unit | |
| | Naum B. Levin | 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *25 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *42-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *42-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This office action is in response to application 10/091,934 and amendment filed on 05/25/2006. Claims 42-48 remain pending in the application. Applicants have amended claims 42 - 44, and added new claims 45-48.

2. By amending claim 42, which necessitates a changing the ground for rejection, and the fact that claims 44, 46 and 48 are dependent from claim 42, the new rejection of claims 42, 44, 46 and 48 was necessitated by applicants' amendment.

By amending claim 43, which necessitates a changing the ground for rejection, and the fact that claims 45 and 47 are dependent from claim 43, the new rejection of claims 43, 45 and 47 was necessitated by applicants' amendment.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 42-48 are rejected under 35 U.S.C. 102(a) as being unpatentable by Goren et al. ("An interconnect-aware methodology for analog and mixed signal design, based on high bandwidth (over 40 GHz) on-chip transmission line approach", Design, Automation and Test in Europe Conference and Exhibition, 2002. Proceedings 4-8 March 2002 Page(s): 804 - 811).

4. As to claims 42-43 Goren discloses:

(42) A method comprising:

when designing an analog and mixed signal integrated circuit, selecting one of a library of pre-defined transmission line topologies for critical interconnect lines (pp 1-2);

(43) An integrate circuit design library comprising:

a set of transmission line topologies for critical interconnect lines capable of carrying analog and mixed signals, which topologies comprise return paths therein (pp 1-3); and

a set of parameterized , equivalent RLC ladder networks, one per topology (pp 1-3).

5. As to claims 44-48 Goren recites:

(44) The method implementing means for performing both frequency and time domain analysis for each transmission line placed into an integrate circuit design (p 4);

(45), (46) The library/method, wherein at least an inductance parameter is a function of frequency (p 4);

(47), (48) The library/method, wherein said frequency ranges from DC to a transistor cut-off frequency (p 4).

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claim 42 is rejected under 35 U.S.C. 102(e) as being unpatentable by Miller et al. (US Patent 6,539,531).

7. As to claim 42 Miller discloses:

(42) A method comprising:

when designing an analog and mixed signal integrated circuit (... suppose an IC has both low frequency analog I/O signals and high frequency digital I/O signals. While a designer also might want the interconnect system conveying the analog signals to provide very low distortion at low signal frequencies and to block high frequency noise, the designer might want the interconnect systems conveying the high frequency digital output signals to have a high bandwidth. Thus, if we use the same interconnect system for each kind of signal, the interconnect system can be a limiting factor in IC design – col.4, ll.50-59), selecting one of a library of pre-defined transmission line topologies (A method for designing integrated circuits (ICs) and their interconnect systems includes IC component cells and interconnect component cells in a cell library. ... each interconnect component cell includes both a physical and behavioral model of a separate internal or external component of an interconnect system that may link the IC to external nodes. Both the IC and its interconnect systems are designed by selecting and specifying interconnections between component cells included in the cell library – Abstract; The model usually depicts the external portions of an interconnect system as a simple transmission line - col.9, ll.21-22) for critical (The interconnect system for each of an IC's terminals, derived from interconnect component cells in accordance with the invention, can be optimized for the particular type of signal – col.13, ll.22-25)

interconnect lines (Abstract; col.4, ll.24-38; col.4, ll.50-67; col.9, ll.21-29; col.10, ll.66-67; col.11, ll.1-22; col.11, ll.37-56; col.13, ll.21-32; col.13, ll.56-67).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 43, 45 and 46 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miller in view of Chang et al. (US Patent 6,381,730).

7. As to claim 43 Miller discloses:

An integrate circuit design library (A method for designing integrated circuits (ICs) and their interconnect systems includes IC component cells and interconnect component cells in a cell library. ... each interconnect component cell includes both a physical and behavioral model of a separate internal or external component of an interconnect system that may link the IC to external nodes. Both the IC and its interconnect systems are designed by selecting and specifying interconnections between component cells included in the cell library – Abstract) comprising:

a set of transmission line topologies for critical interconnect lines (The interconnect system for each of an IC's terminals, derived from interconnect component cells in accordance with the invention, can be optimized for the particular type of signal

– col.13, ll.22-25) capable of carrying analog and mixed signals (... suppose an IC has both low frequency analog I/O signals and high frequency digital I/O signals. While a designer also might want the interconnect system conveying the analog signals to provide very low distortion at low signal frequencies and to block high frequency noise, the designer might want the interconnect systems conveying the high frequency digital output signals to have a high bandwidth. Thus, if we use the same interconnect system for each kind of signal, the interconnect system can be a limiting factor in IC design – col.4, ll.50-59) (Abstract; col.4, ll.24-38; col.4, ll.50-67; col.9, ll.21-29; col.10, ll.66-67; col.11, ll.1-22; col.11, ll.37-56; col.13, ll.21-32; col.13, ll.56-67).

With respect to claim 43 Miller describes the features above but lacks an integrate circuit design library further comprises a set of parameterized RLC ladder networks, one per topology, and wherein topologies comprise return paths.

As to claim 43 Chang recites:

An integrate circuit design library comprising:

a set of parameterized (A parasitic extractor analyzes structures within a selected distance of a selected conductor within the integrated circuit and determines parasitic inductance values for the selected conductor using the parameterized inductance function of the interconnect primitive library – Abstract; The present invention provides a comprehensive system for generating accurate RLC models for interconnect lines – col.3, ll.66-67; Interconnect library builder 301 then repeats the above process for several different conductor widths and conductor spacings, in each case assuming that the conductors of primitive 1000 are identical in width and uniform in spacing.

Interconnect library builder 301 thereby creates a parameterized inductance function - col.7, ll.28-33), equivalent RLC ladder networks (FIG. 7 shows an RLC network 700 output by RLC network module 404 for a regular line segment. As shown in FIG. 7, the resistance and inductance calculated for the line segment are formed as a resistor 704 and an inductor 712 connected in series. All individual coupling capacitances (converted to ground capacitances) are combined and equally split into capacitors 706 and 708, ... In FIG. 8, the "T" junction resistance is divided into three equal resistances 802, 804, 806. ... The inductance calculated for the "T" junction is represented by three equal inductors 808, 810, 812 – col.17, ll.20-50), one per topology (Abstract; col.3, ll.9-20; col.3, ll.66-67; col.4, ll.1-4; col.5, ll.10-24; col.7, ll.5-65; col.10, ll.19-28; col.16 ll.37-51; col.17, ll.20-50; claim 1); and

wherein topologies comprise return paths (Interconnect library builder 301 thereby creates a parameterized inductance function in which the parameters or independent variables are the conductor width and the conductor spacing. Since the signal path and closest return path are assumed to be adjacent conductors, the parameters for the inductance function are in effect the conductor width and the distance to the closest return path col.7, ll.32-38) (col.7, ll.5-65; claim 1).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Chang's teaching regarding the integrate circuit design library further comprises a set of parameterized RLC ladder networks, one per topology, and wherein topologies comprise return paths and use it in Miller's invention to improve an accuracy of the parasitics analysis, by estimating of the RLC ladder networks for the

networks for the critical nets not based on a simple model which often takes into account only the dimensions of individual transmission lines, but involving parameterized RLC function and return path in estimating of the RLC ladder networks, thereby improving the analog and mixed signal integrated circuit design.

8. As to claims 45-46 Chang describes:

(45), (46) The library/method, wherein at least an inductance parameter is a function of frequency (col.4, ll.43-56; col.7, ll.5-17; col.16, ll.37-51).

9. Claim 44 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miller in view of Suaya et al. (US Pub. No.: 20030131334).

As to claim 44 Suaya discloses:

(44) The method implementing means for performing frequency and time domain analysis for each transmission line placed into an integrated circuit design ([0067]-[0069]; [0141]).

10. Claims 46 and 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miller in view of Chang and further in view of Tsividis Y. ("Mixed analog-digital VLSI devices and technology", 1995, pp 1-284).

With respect to claims 46 and 47 Miller in view of Chang describes the features above but lacks an integrated circuit design library, wherein frequency ranges from DC to a transistor cut-off frequency.

As to claims 46 and 47 Tsividis teaches:

The library/method, wherein said frequency ranges from DC to a transistor cut-off frequency (p 112, pp 120-126, pp 147-191, pp 205-250).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Tsividis' teaching regarding the integrated circuit design library, wherein frequency ranges from DC to a transistor cut-off frequency and use it in Miller's and Chang's invention to improve an accuracy and reliability of the parasitics analysis in the integrated circuits with very high bandwidth of frequencies, even if frequency equals zero (DC), thereby improving the analog and mixed signal integrated circuit design.

## ***REMARKS***

11. The examiner introduces a new ground of rejection that is necessitated by applicant's amendment of the claims, see ***Form Paragraph 7.42.031*** (¶ 7.42.031 Action Is Final, Action Following Submission Under 37 CFR 1.129(a) Filed On Or After June 8, 2005).

12. Accordingly, **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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VUTHE SIEK
PRIMARY EXAMINER